In the Specification

Amend the following numbered paragraphs of the specification:

[0019] Fig. 2 is a schematic block diagram representation according to a first embodiment of the invention showing a portion of a memory array, wherein an existing external signal "read cycle n+1" is combined with a "conventional precharge signal" in an AND-gate thereby generating a new precharge signal for a respective array segment; and

[0023] Referring again to Fig. 1, the broken lines in the bitline true (BLT) and bitline complement (BLC) timing signatures show the benefit achieved by the present invention. Namely, that the bitlines are not precharged when a write access follows a read or write access. For example, broken lines A and B in the BLT and BLC signals indicate that the bitlines are not precharged when a write access follows after a read access as further indicated by broken line C. However, benefits can only be achieved when the data, associated with that specific bitlines does not change its value from cycle n to cycle n+1. Thus, no power savings between t4 and t5 are achievable.

[0031] While the invention has been described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is understood that ~~numerour~~ numerous other modifications and variations can be ~~dfevised~~ devised without departing from the scope of the invention.

In the Abstract

Amend the abstract as follows:

~~The present invention relates to computer hardware and in particular to power management of high frequency storage designs, which are able to implement differential write or read access in a dynamic hardware arrangement of storage cells having some inner segmentation. More particularly, the present invention relates to a~~ A method and ~~respective~~ system of accessing memory cells within a dynamic hardware memory block operated with a bitline precharge circuit, in which differential read/write access operations are performed by activating complementary bitlines. A reduction in power dissipation is realized by determining whether ~~an~~ a next access operation following a current access operation is a read or write access, and performing a precharge of the bitlines of the array only when a read operation follows the current access operation. A

conventional precharge control signal ~~(20)~~ is combined with an external control signal ~~(22)~~ indicating if the next cycle is a read cycle. The combination of the two signals can be used, for example, as input to a simple AND gate to generate an effective precharge signal ~~(24)~~. The effective precharge signal permits precharging of bitlines only when those bitlines are used for read access in a respective next cycle. ~~(Fig. 2)~~

In the Drawings

The Examiner objected to the drawings under 37 CFR 1.83(a) as failing to show every feature of the invention specified in the claims. Accordingly, Applicants have amended Fig. 2 to include a more complete schematic representation of the system and method claimed herein. A proposed set of drawings is attached as Appendix A to this amendment to overcome the Examiner's objections. Following the Examiner's approval of the form of the proposed drawings, Applicants will submit a formal set of drawings that will comply in all respects with 37 CFR 1.83.

The Examiner also objected to the drawings under 37 CFR 1.83(a) as failing to show every feature of the invention as specified in the claims. Specifically, the examiner objected to the failure to include a "multiplexer" logic function in the drawings, as recited in claim 10. Applicants respectfully submit that the term "multiplexer" is defined in the IBM Dictionary of Computing, McGraw Hill, 1994, compiled and edited by George McDaniel, and is a term readily understood and recognized by a person of ordinary skill in the art. Further, a person of ordinary skill in the art would understand that a multiplexer may be configured to implement a combinatorial logic function, such as an AND gate. Moreover, Applicants' specification at paragraph 0023 indicates that "the combination of the two signals 20 and 22 to generate the effective precharge signal 24 is not restricted to an AND gate, but can also be realized by other logic implementations."

Applicants have amended the drawings to illustrate the memory array components coupled to a logical AND element to produce a precharge control signal based on an external read cycle